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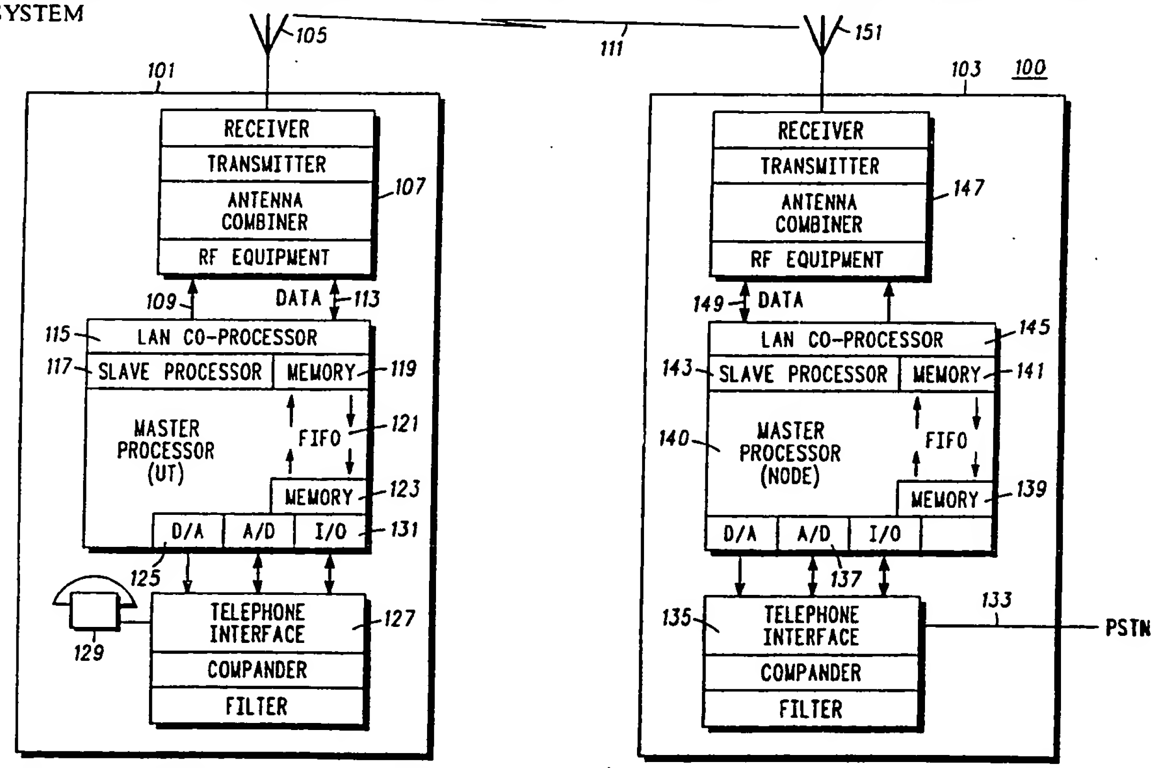
(54) Title: DISTRIBUTED SYNCHRONIZATION METHOD FOR A WIRELESS FAST PACKET COMMUNICATION SYSTEM



(57) Abstract

A distributed synchronization method for a wireless fast packet communication system (100) is disclosed. The distributed synchronization method, according to the invention, provides for the combination of both voice and data in a single switch using a common packet structure. It allows for the dynamic synchronization of packets. This includes not only bandwidth within the

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DISTRIBUTED SYNCHRONIZATION METHOD FOR A WIRELESS FAST PACKET COMMUNICATION SYSTEM

Technical Field

This invention pertains to voice/data packet switches and, more particularly, to a distributed synchronization method for a wireless fast packet communication system.

Background of the Invention

Voice and data switches are known in the prior art. Packet switching is also known. In the past, however, synchronization for the control of the devices sending and receiving information packets in a voice/data packet switch has been a problem. This problem has been related to the problem of dynamically allocating the packet bandwidth between the various peripheral devices attached to the switch for voice information and data information. Another related factor has been the network interface architecture for the switch. The network interface architectures of past switches have used the same bus for both data and control. When coupled with the problem of dynamically allocating bandwidth on the bus, this network interface architecture has resulted in the switch having a low switching capacity and throughput. In PBX's, it is because all data is switched byte-by-byte. In data packet switches, it is a processor horsepower issue. These performance problems become even more significant in the context of modern fast packet protocols. It

would be desirable, therefore, to provide a voice/data packet switch with an improved architecture.

Key to this packet switch architecture is a method for achieving synchronization of packets transmitted between the various nodes and user terminals. A failure to achieve this goal will likely result in instances of unacceptable reception coherence, usually caused by carrier frequency differentials, deviation control differences, phase differentials with respect to the modulation signal, and the like.

Summary of the Invention

It is an object of the present invention, therefore, to provide an architecture for a wireless fast packet communication system. It is a further object of the present invention to provide a method for achieving synchronization of packets transmitted between the various nodes and user terminals in such a system.

Accordingly, a distributed synchronization method for a wireless fast packet communications system is disclosed. The distributed synchronization method, according to the invention, provides for the combination of both voice and data in a single switch using a common packet structure. It allows for the dynamic synchronization of packets. This includes not only bandwidth within the voice or data areas of the frame, but also between the voice and data portions.

Brief Description of the Drawings

Fig. 1 is a block diagram that shows a first embodiment of a wireless fast packet communication system, according to the invention.

Fig. 2 shows a frame for the first embodiment.

Fig. 3 shows the voice/fixed data area within the frame.

Fig. 4 shows the packetized data area within the frame.

Fig. 5 shows a typical network topology for the first embodiment.

Fig. 6 shows a first synchronization timing diagram for the first embodiment.

Fig. 7 shows a second synchronization timing diagram for the first embodiment.

Table A shows the code for accomplishing the synchronization method, according to the invention.

Detailed Description of the Invention

Fig. 1 is a block diagram that shows a first embodiment 100 of a wireless fast packet communication system, according to the invention. There is shown a node 103 and a user terminal (UT) 101. It will be appreciated by those skilled in the art that a multiplicity of UT's may be used. However, for simplicity only one is shown in Fig. 1.

The following is a description of the node 103's processing of the voice signal from the PSTN 133 to the RF channel 111:

The voice input from the PSTN 133 is compressed and filtered by the telephone interface 135, and forwarded to the A/D 137 for digitization. From there, it is placed into voice packets in the local memory 139 of the master processor 140 and forwarded by the master processor via the FIFO into the local memory 141 of the slave processor 143. There the slave processor gives the packet to the LAN co-processor 145 for serialization to the RF equipment 147, and the LAN co-processor converts it into a serial data stream 149. The RF equipment 147, comprising a receiver/transmitter/antenna combiner, creates an RF signal and feeds it to the RF antenna 151.

The software contained within the LAN board and the software contained within the master processors in the computer systems perform all of the above and following functions.

The following is a description of the UT 101's processing of the voice signal from the RF channel 111 to the telephone 129:

The UT 101 includes an RF antenna 105 connected to a receiver/transmitter/antenna combiner 107. Power and control of the RF

equipment is performed by wires 109. The RF equipment 107 receives a serial data stream from the RF signal 111, and feeds the serial data stream 113 to a LAN co-processor 115. Within the computer system, a LAN board (which contains the LAN co-processor 115, slave processor 117, and its associated local memory 119) receives the data stream and converts it into voice packets into the local memory 119 of the slave processor 117. The slave processor then strips and forwards the voice packets using the FIFO 121 to the master processor's local memory 123 for reconstruction into voice using software contained within the computer system using the D/A converter 125 in the computer system. The telephone interface 127 expands and filters the outgoing analog voice signal, and presents it to the telephone 129. Additionally, local ringing of the telephone 129 is accomplished by fast data packets being processed in common by the above system up to and including the master processor memory unit 123, and then the Master processor places the ring indication in the I/O port 131, which is then fed to the telephone interface 127 and forwarded to the telephone 129.

There will be a repetitive frame occurring periodically, which contains the bi-directional signalling and packet data necessary for the correct operation of the system. This frame 200 is shown in Fig. 2. Within the voice/fixed data area, there are a number of time slots (A-H) allocated to fixed rate data and voice, and are assigned without collision by the node. Within the packetized data area, each device is free to broadcast at any time, and is responsible for detecting collisions.

Within the voice/fixed data area, the format shown in Fig. 3 applies.

Within the packetized data area, the format shown in Fig. 4 applies.

Each transmission within a frame may be encoded in order to improve the accuracy of the received data. If this code utilizes several

copies of the original data, the arrival times of similar packets may be different. In this case, an algorithm in software compensates for the different arrival times.

This system allows for maximum spectral efficiency by allocating the required bandwidth to each of the users of the common communications path. As mentioned above, previous systems did not allocate the bandwidth on a need basis, but rather allocated the bandwidth at system start-up. As a result, this system takes advantage of the fast packet switching technology that allows both circuit and non-circuit connections to be made in the same system.

Fig. 5 shows a typical network topology 500 for the first embodiment. There is shown a multiplicity (n) of nodes, N_1 through N_n. There is also shown a multiplicity (n) of terminals T_1 through T_n. The nodes communicating with each other and with the terminals on a shared communications path via a fast-packet-switched mechanism, the fast-packet-switched mechanism being controlled by a bandwidth allocation scheme preventing collision between the various units that may be accessing the common communications path.

The basic process of obtaining frame synchronization between two Network Interface (NI) units is really quite simple. To start, let us assume that one unit is "master" and is transmitting exactly one frame sync packet in each frame. This packet must contain the "time-of-frame" that it is transmitted, as counted in bytes from the start of the NI data area to the first byte of the header (first byte following the end of the packet synch sequence). The approximate location of this packet in the frame must be known at the receiver in order to meet the requirements for unconditional stability during the initial portion of the sequence. There is only one other significant complication -- the process used for initial sync acquisition must allow for the interference caused by the receiver commands in the NI control memory.

The receiver's action is actually quite simple -- it extracts the time-of-transmission described above, and compares it to the reception-time

stamp provided by the NI, adjusting for propagation delays in the buffers and communications equipment. Assuming there is a significant error, it must then determine the proper direction to shift its NI to find sync in the shortest time; the required adjustment will always be between a negative 1/2 and a positive 1/2 frame.

This total computed error is then divided by a stability factor such as, for example, 16, to preserve stability in the situation where one device may be receiving several other unsynchronized devices. Further checks are then made to allow for the limit case and to limit the adjustment to whole words (even addresses only) as required by the current Network Interface design.

The overall scheme also allows for determining the exact instant when synchronization is acquired, and a (fairly slow) determination of lost sync. This is accomplished by creating a global variable 'in_sync'. This variable is decremented by one (with a lower limit of zero) on every frame start interrupt, and is incremented by 16 (up to an upper limit that depends on the system size such as, for example, 400) every time a frame sync packet is processed that requires no adjustment to the frame time; that is, every time frame sync is determined to be perfect. When 'in_sync' is zero, the system is out of sync.

The code for accomplishing both these algorithms is shown in Table A.

The remaining problem with sync acquisition revolves around the repeated enable commands required by the receiver to control packet sync falsing. The receiver-enable command sequence is designed to abort the process of receiving a packet, if it occurs during the packet. One way of achieving this is to require that every frame contain a "receiver enable" sequence consisting of the following commands:

- Everybody clear the bus;
- Receiver enable;
- Select antenna;
- Set NI as bus destination;
- Set radio as bus source.

When the packet sync detector falses, it will be reset when it encounters the above sequence, or when the NI realizes that it has been handed a data sequence that does not represent a valid header (when the header CRC check fails).

The problem that arises can be seen in Fig. 6. The problem occurs when the first sync packet is decoded, if the receiving device's clock is slightly faster than the node's (this, of course, will be the case one-half of the time). The computed adjustment would move the receiving frame to the left, and thus put the control sequence right on top of the next received sync packet. This packet will be missed, and normal drift will move succeeding receive frames to the right until the control sequence occurs after the sync packet. At this time, another sync packet will be received, an adjustment to the left computed, and the sequence repeated. Thus, the net effect is to line the control sequence up with the sync packet, rather than to align the frames.

The solution is simple -- put the control sequence exactly one-half frame away from the expected time of the sync packet. This is shown in Fig. 7.

In this case, the first packet will probably not be received. However, the relative frame times will soon drift, and no matter which way the relative position of the receiver moves, the first packet received will result in a correction in the proper direction to move the control sequence away from the packet, since it will be in the direction of the smallest required change.

Once frame sync is acquired, the above control sequence will of course be removed, and the operating framework substituted.

Once approximate frame sync has been achieved by all devices, each device in the system (all nodes, UIM's and NIM's) will continue to synchronize on the average of all the frame clocks it can see, including its own. This concept results in the best overall timing performance, and therefore in the smallest required guard times between packets from different devices. For example, a chain of four nodes could exhibit a frame-time difference of 6 bytes from the first to the last; the average

difference will depend on the relative free-running clock frequencies of the 4 NI's involved, and could well remain at the worst case stated above.

The averaging method, on the other hand, will cause the average difference to stay at zero.

An additional consideration is fallback -- the appropriate action to take in the event of a failure. For example, if the system consists of 3 nodes, and the second slaves to the first, and the third to the second, what happens when the second fails? If sync control is by priority, this failure must be detected and the priority adjusted accordingly if the system is not to fall out of sync. On the other hand, the averaging scheme automatically adjusts accordingly.

The clocks may, for example, have a frequency accuracy of 5 parts per million. For a frame size of 3750 bytes, this means a maximum slip of:

$$2 * 5 * 10^{-6} * 3750 = 0.0375 \text{ bytes per frame}$$

for two clocks that are as far apart as possible (one at the high end of the spec, the other at the low end). This means that a one-word adjustment will be required once every 27 frames in this limit case.

There are several potential solutions to the problem of obtaining initial synchronization among several nodes in a large system. Perhaps the simplest is to define an order of priority, and allow each node to start transmitting only after it has heard and locked to the unit next higher in the priority structure. This has the appeal of being very simple to design, but requires that each node "know" the identity of its immediate superior in the structure. There is the additional problem of determining the proper action if the superior is never heard. This may make failure recovery more difficult.

The available variables in each node include both frame phase and absolute frame rate (the frame size can be varied over quite wide limits, and need not be fixed at the "system" rate until overall sync is obtained). A properly-chosen random-number-based frame rate and phase will almost certainly provide an adequate initialization procedure, as long as the random number generators in the various nodes can be

seeded with different numbers, to avoid identical actions from an identical starting point, such as might be provided by recovery from a major power failure. This requirement may be met by the inclusion of an electronic serial number in each unit.

In one frame structure, for instance, each node sends a frame-sync packet on each sector in every frame. However, it is adequate if each node/sector radiates a frame-sync on every 4th frame. This would allow UIM/NIM's to re-evaluate their local antenna selection once every 24 frames (48 ms), and would allow a worst-case frame-sync timing update of once every 24 frames, well within the 27-frame worst-case limit calculated earlier.

This reduction in frame-sync packets implies that a more efficient frame design can be accomplished, at the cost of the software required to change the "fixed" portion of data in NI data buffer at the end of each frame. To this end, it might be advantageous to put the node transmissions at the end of the frame, and the UIM/NIM transmissions at the beginning, to simplify the software timing considerations.

While various embodiments of a distributed synchronization method for a wireless fast packet communication system, according to the present invention, have been described hereinabove, the scope of the invention is defined by the following claims.

What is claimed is:

Claims:

1. A distributed synchronization method for a wireless fast packet communications system, said system including a master unit transmitting one frame sync packet in each frame, said method comprising the steps of:

at said transmitter:

(a) including in said packet an indication of the time-of-frame that it is transmitted, as counted in bytes from the start of the NI data area to the first byte following the end of the packet sync sequence;

at said receiver:

(b) extracting said time-of-transmission indication;

(c) comparing said indication to a reception-time stamp, said reception stamp related to the time of receipt of said packet;

(d) adjusting for propagation delays;

(e) determining when there is significant error;

(f) adjusting said NI data area to find sync in the shortest time.

2. A distributed synchronizer for a wireless fast packet communications system, said system including a master unit transmitting one frame sync packet in each frame, said synchronizer comprising:

at said transmitter:

(a) means for including in said packet an indication of the time-of-frame that it is transmitted, as counted in bytes from the start of the NI data area to the first byte following the end of the packet sync sequence;

at said receiver:

(b) means for extracting said time-of-transmission indication;

(c) means for comparing said indication to a reception-time stamp, said reception stamp related to the time of receipt of said packet;

(d) means for adjusting for propagation delays;

(e) means for determining when there is significant error;

(f) means for adjusting said NI data area to find sync in the shortest time.

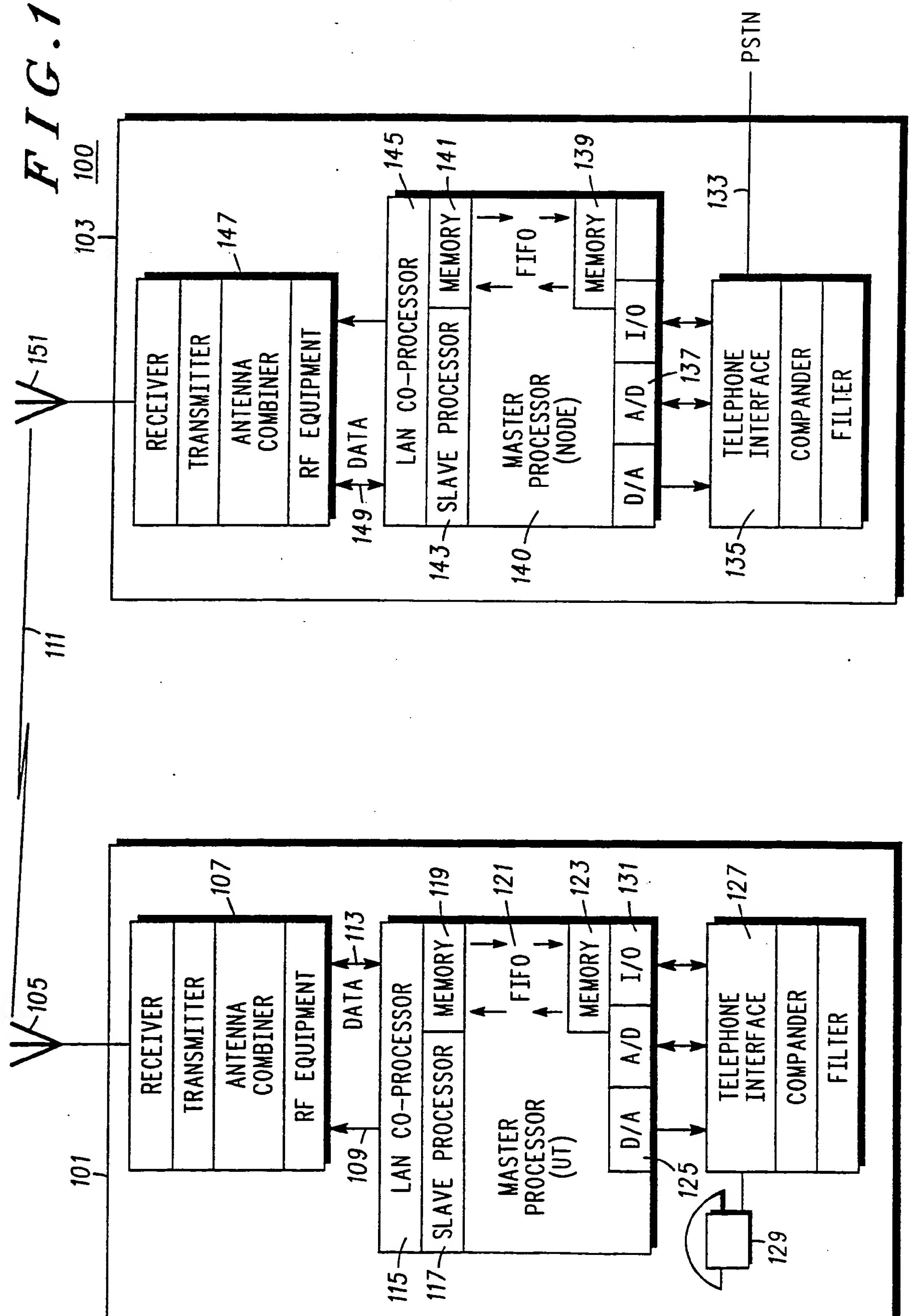
100
103
RECEIVER
TRANSMITTER
ANTENNA COMBINER
RF EQUIPMENT
147
151
DATA
149
LAN CO-PROCESSOR
145
MEMORY
141
SLAVE PROCESSOR
143
FIFO
MEMORY
139
MASTER PROCESSOR (NODE)
140
D/A
A/D
I/O
137
TELEPHONE INTERFACE
COMPANDER
FILTER
133
135
PSTN
111
101
105
RECEIVER
TRANSMITTER
ANTENNA COMBINER
RF EQUIPMENT
107
109
DATA
113
LAN CO-PROCESSOR
115
MEMORY
119
SLAVE PROCESSOR
117
FIFO
121
MEMORY
123
MASTER PROCESSOR (UT)
D/A
A/D
I/O
131
125
TELEPHONE INTERFACE
COMPANDER
FILTER
127
129

FIG.1

FIG. 2

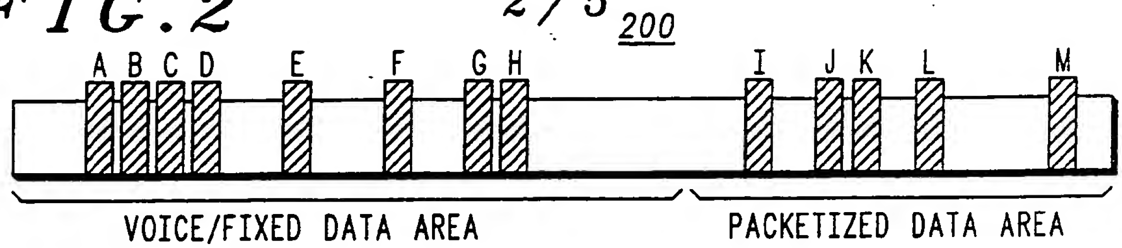

FIG. 3

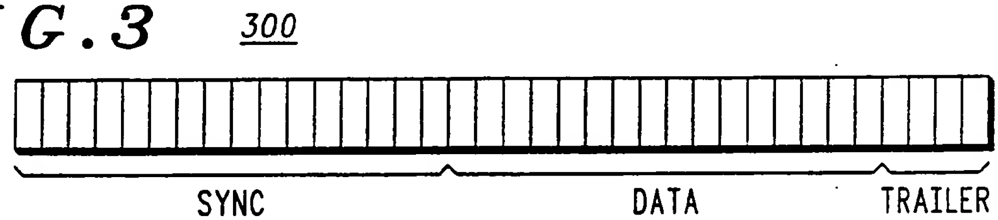

FIG. 4

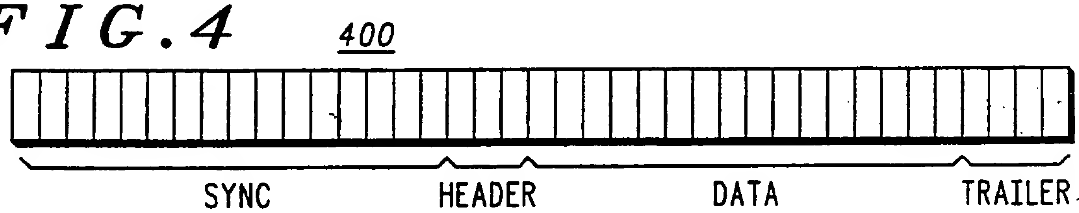

FIG. 5

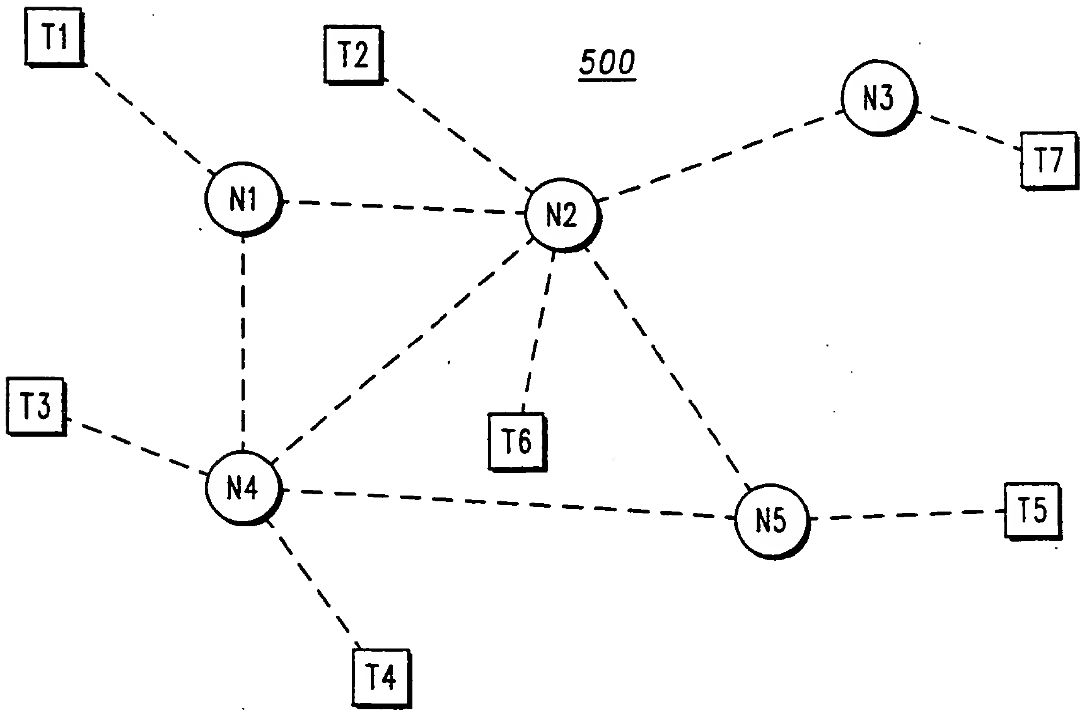

FIG.6

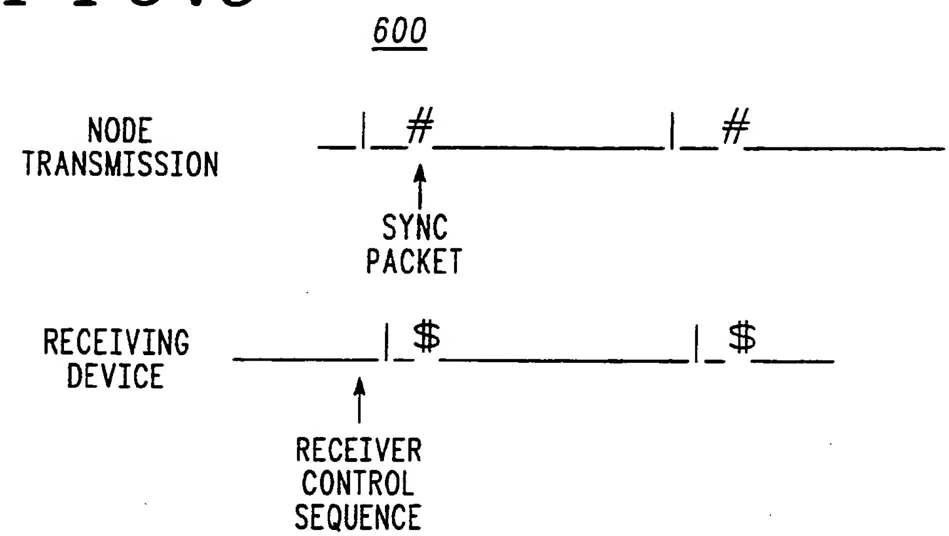
600
NODE TRANSMISSION
#
#
SYNC PACKET
RECEIVING DEVICE
$
$
RECEIVER CONTROL SEQUENCE

FIG.7

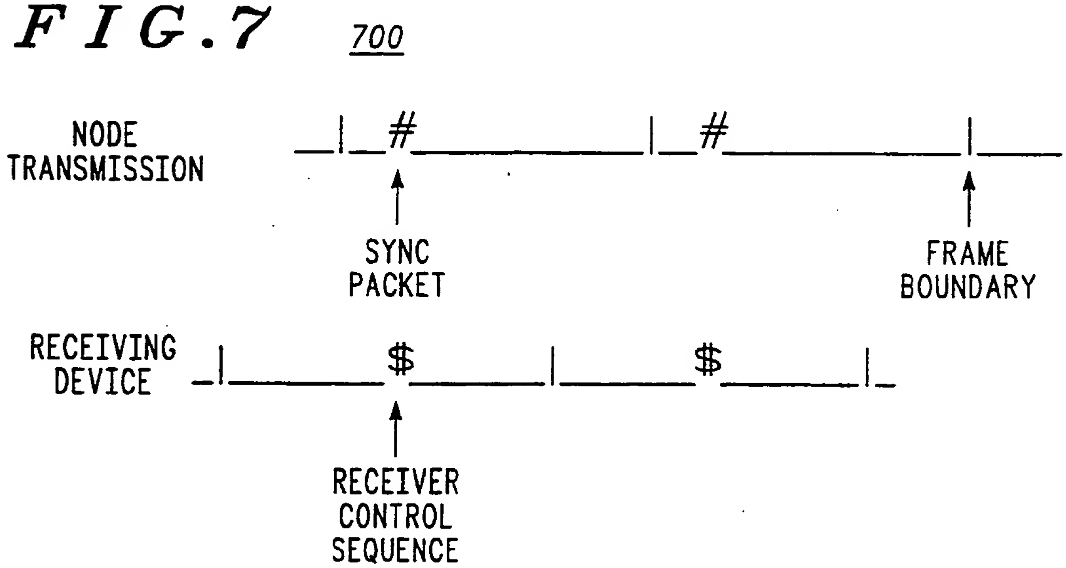
700
NODE TRANSMISSION
#
#
SYNC PACKET
FRAME BOUNDARY
RECEIVING DEVICE
$
$
RECEIVER CONTROL SEQUENCE

FIG. 8-1 TABLE A

```
/*  SYNC_ADJUST(DIFF) IS THE FUNCTION THAT IMPLEMENTS THE
    FRAME OFFSET ADJUSTMENT.

    FRAME_OFFSET IS THE TIME-OF-FRAME TRANSMITTED IN THE
    SYNC PACKET

    TM_STAMP IS THE TIME STAMP SUPPLIED BY THE NI

    OFFSET_CONSTANT IS THE COMPUTED BUFFERING AND PROPAGATION
    DELAY FOR ONE DIRECTION IN THE RADIO CHANNEL. IT IS
    EQUAL TO 6 BYTES IN THE CURRENT HARDWARE.

    FRAMESIZE IS THE SIZE OF THE FRAME IN BYTES

    IN_SYNC IS A GLOBAL VARIABLE THAT TELLS THE SYSTEM WHEN
    IT IS IN FRAME SYNC--WHILE IN_SYNC IS NON-ZERO, THE
    SYSTEM IS IN FRAME SYNC. IN_SYNC IS DECREMENTED BY ONE
    ON EVERY FRAME INTERRUPT, AND IS INCREMENTED BY 16 EACH
    TIME A FRAME-SYNC PACKET REQUIRES NO ADJUSTMENT OF FRAME TIME.

*/
{
 DIFF = FRAME_OFFSET - TM_STAMP + OFFSET_CONSTANT;
                          /*COMPUTE THE CURRENT ERROR*/
 IF ((DIFF > 1) || (DIFF < 1)) /*THIS BLOCK IS EXECUTED
              ONLY IF THE ERROR REQUIRES ADJUSTMENT*/
     {
     /*FIRST MAKE SURE THAT IT IS NOT MORE NEGATIVE
       THAN ONE-HALF A FRAME*/
     IF (DIFF > FRAMESIZE / 2)
          DIFF -= FRAMESIZE;
     /*OR THAT IS NOT MORE POSITIVE THAN ONE-HALF
       A FRAME*/
     ELSE IF (DIFF < -FRAMESIZE / 2)
          DIFF += FRAMESIZE;
     DIFF_TMP = DIFF;     /*KEEP THIS SO AS TO KEEP THE
            SIGN*/
     DIFF = DIFF / 16;     /*DIVIDE BY THE STABILITY
                   CONSTANT*/
```

```
        /*NOW MAKE SURE THAT THE RESULT IS A
          POSITIVE MUNBER; THAT IS, MOD IT BYNTHE FRAME
          SIZE*/
        WHILE (DIFF < 0)
            DIFF += FRAMESIZE;

        /*NOW ALLOW FOR THE CASE WHERE THE ERROR WAS
          SIGNIFICANT (ABSOLUTE ERROR GREATER THAN 1
          BYTE) BUT WAS ROLLED TO ZERO BY THE DIVISION*/
        IF (DIFF == 0)
        {
            /*IF THE ORIGINAL DIFF WAS NEGATIVE, MAKE
              THE ADJUSTMENT A NET NEGATIVE ONE WORD*/
            IF (DIFF_TMP < 0)
                DIFF = FRAMESIZE - 2;
        }
        /*NOW MAKE SURE IT IS AN EVEN ADDRESS */
        IF (DIFF % 2)
        {
            /* IF IT IS VERY LARGE (RESULTING IN A
               NEGATIVE ADJUSTMENT) MAKE IT ONE MORE
               NEGATIVE*/
            IF (DIFF > FRAMESIZE / 2)
                DIFF -= 1;
            /*OTHERWISE MAKE ONE LARGER*/
            ELSE
                DIFF += 1;
        }
        /*NOW MAKE THE ADJUSTMENT*/
        SYNC_ADJ(DIFF);
}
/*IF THERE WAS NO ADJUSTMENT REQUIRED, INCREMENT THE
  SYNC CONTROL VARIABLE*/
ELSE IF (IN_SYNC < 400)
    IN_SYNC += 16;
}
```

FIG.8-2

INTERNATIONAL SEARCH REPORT

International Application No PCT/US90/06011

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC5 H04J 3/06, H04J 3/26
US CL. 370/100.1, 103,94.2

II. FIELDS SEARCHED

Minimum Documentation Searched

Classification System	Classification Symbols
US CL.	370/100.1, 103,94.2, 105.1

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched

III. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
Y,P	U.S., A 4,894,823(ADELMANN ET AL.)16 January 1990 See column 8, lines 14-31, and columns 19-30.	1,2
Y	U.S., A 4,519,068 (KREBS ET AL.) 21 May 1985 See figure 2, and column 3 line 59 through column 4, line 19	1,2
Y	U.S. A 4,748,623 (FUJIMOTO) 31 May 1988 . See entire document	1,2
A	U.S. A 4,525,832 (MIYAO) 25 June 1985 See entire document	1,2
A	U.S. A 4,530,091 (CROCKETT) 16 July 1985 See entire document	1,2
A	U.S. A 4,670,871 (VAIDYA) 02 June 1987 See entire document	1,2
A	U.S. A 4,679,188 (FUKUDA ET AL) 07 JULY 1987 See entire document	1,2

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
28 FEBRUARY 1991	02 APR 1991
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ISA/US	Veronica ... for MIN JUNG